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EXAMINER	
PHAM, THANHHA S	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/244,788	PARIKH, SUKETU A.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sh t with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-13,15-19 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-13,15-19 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action responses to Applicant's Amendment in Paper No. 17 dated 12/18/01.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 19 and 23-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19, line 28, "additionally forming a third and fourth via pattern" renders the claim indefinite. It is not clear how a third and fourth via patterns are formed and are located.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1, 9 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al [US 5,976,972].

With respect to claim 1, Inohara et al, figs 28-32 and col 1-19, discloses the claimed method of forming a structure on a substrate, the method comprising:

a) depositing a first dielectric layer (43, fig 28, col 13 lines12-18) on the substrate (combination structure of 41/42/54);

b) depositing a second dielectric layer (44, fig 28, col 13 lines 12-18 & 62-67) on the first dielectric layer, wherein the first and second dielectric layer comprise materials having dissimilar etching characteristics (the second layer 44 being selectively etched with respect to the first dielectric layer 43);

c) depositing a first mask layer (56, figs 28 and 38, col 13 lines 19-24 and col 14 lines 50-58) over the second dielectric layer wherein the first mask layer includes a first via pattern having a width T;

d) anisotropically etching the first via pattern through the second dielectric layer (figs 28 and 39, col 13 lines 19-24 and col 14 lines 59-65);

e) removing the first mask (fig 28);

f) depositing a third dielectric layer (45, fig 29, col 13 lines 24-29) on the second dielectric layer, wherein the second and third dielectric layers comprise material having dissimilar etching characteristics (fig 30 shows the third dielectric layer 45 is etched while the second dielectric layer 44 is not);

g) depositing a second mask layer (47, fig 29, col 13 lines 24-36) on the third dielectric, wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P such that T exceeds P a measure M;

h) anisotropically etching the trench pattern through the third dielectric layer, thereby forming (1) a first trench in the third dielectric layer and (2) a second via pattern (fig 30, col 13 lines 39-48);

i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the substrate (via hole 48 reaching toward the substrate, figs 30 & 31, col 13 lines 39-53); and

j) anisotropically etching the first trench through the second dielectric layer, thereby forming a second trench extending through the second and third dielectric layers, wherein the via hole and the second trench are adapted for fabricating a dual damascene structure (fig 31, col 13 lines 39-53 and col 10 lines 10-18).

- With respect to claim 9, Inohara et al (figs 28 and 38, col 13 lines 19-24 and col 14 lines 50-58) discloses that depositing the first mask (56, photoresist mask)

comprises depositing a mask layer selected from the group consisting of photoresist mask layers, hard mask layers and combinations of photoresist mask layer and hard mask layer.

- With respect to claim 11, Inohara et al (fig 32, col 13 lines 54-61) discloses simultaneously filling the second trench (46) and the via hole (48) with a conductive material whereby a dual damascene structure is formed.

2. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al [US 5,976,972].

Inohara et al, figs 28-31 and col 1-19, discloses the claimed method of forming a structure on a substrate (41) including at least one interconnect line (42), the method comprising:

a) depositing a first dielectric layer (43, fig 28, col 12 lines 4-8) on the substrate (41) such that there is no material layer interposed between the interconnect line (42) and the substrate (41);

b) depositing a second dielectric layer (44, fig 28, col 13 lines 12-18 & 62-68) on the first dielectric layer, wherein the first and second dielectric layer comprise materials having dissimilar etching characteristics (the second layer 44 being selectively etched with respect to the first dielectric layer 43, see fig 28);

c) depositing a first mask layer (56, figs 28 and 38, col 13 lines 19-24 and col 14 lines 50-58) over the second dielectric layer wherein the first mask layer includes a first via pattern having a width T;

d) anisotropically etching the first via pattern through the second dielectric layer (figs 28 and 39, col 13 lines 19-24 and col 14 lines 59-65);

e) removing the first mask (fig 28);

f) depositing a third dielectric layer (45, fig 29, col 13 lines 24-29) on the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics (fig 30 shows the third dielectric layer 45 is etched while the second dielectric layer 44 is not) and wherein the first and third dielectric layers comprises materials having similar etching characteristics (fig 30 and col 13 lines 39-48 show the first dielectric layer 43 and the third dielectric layer 45 are etched by RIE);

g) depositing a second mask layer (47, fig 29, col 13 lines 24-36) on the third dielectric, wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P such that T exceeds P a measure M;

h) anisotropically etching the trench pattern through the third dielectric layer, thereby forming (1) a first trench in the third dielectric layer and (2) a second via pattern (fig 30, col 13 lines 39-48);

i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the substrate (via hole 48 reaching toward the substrate, figs 30 & 31, col 13 lines 39-53); and

j) anisotropically etching the first trench through the second dielectric layer, thereby forming a second trench extending through the second and third dielectric

layers, wherein the via hole and the second trench are adapted for fabricating a dual damascene structure (fig 31, col 13 lines 39-53 and col 10 lines 10-18).

3. Claims 19, 23, and 28-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin [US 6,093,632].

- With respect to claim 19, Lin, figs 4-8 and col 1-6, substantially discloses the claimed method of forming a structure on a substrate comprising step of:

a) depositing a first dielectric layer (3, fig 4, col 5 lines 10-28) on a substrate (1/2);

b) depositing a second dielectric layer (10a, fig 4) on the first dielectric layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics (the first dielectric layer comprising silicon oxide 4 having dissimilar etching characteristics to the second dielectric layer 10b comprising silicon nitride, the first dielectric layer being etched selectively to the second dielectric layer – see col 5 lines 56-66);

c) depositing a first mask layer (11, fig 5, col 5 lines 29-34) on the second dielectric layer wherein the first mask includes:

[1] a first via pattern having a width WV1 (see first opening between the first mask layer 11 being counted from left to right, fig 5),

[2] a second via pattern having a width WV2 (see the third opening between the first mask layer 11 being counted from left to right, fig 5), and

[3] a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS (see the second opening between the first mask layer 11 being counted from left to right, fig 5);

d) anisotropically etching the first and second via patterns through the second dielectric layer and forming a sacrificial etch segment by simultaneously anisotropically etching the sacrificial etch pattern through the second dielectric layer (see fig 5, col 5 lines 29-34);

e) removing the first mask layer (see fig 6, col 5 lines 43-45);

f) depositing a third dielectric layer (13, fig 6, col 5 lines 44-48) on the second dielectric layer (10b), wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics (the third dielectric layer 13 comprising silicon oxide having dissimilar etching characteristics to the second dielectric layer 10b comprising silicon nitride, the third dielectric layer being etched selectively to the second dielectric layer – see col 5 lines 56-66);

g) depositing a second mask layer (14, fig 6) on the third dielectric layer (13), wherein the second mask includes:

[1] a first trench pattern overlaying the first via pattern and the third dielectric layer, and having a width WT1(see fig 6, the left trench opening 15a in the second mask 14 that overlays the first via pattern 12a and the third dielectric layer 13), and

[2] a second trench pattern having a width WT2 overlaying the second via pattern and the third dielectric layer (see fig 6, the right trench opening 15a in

the second mask 14 that overlays the "second" via pattern 12a (the third opening between the first mask layer 11 being counted from left to right) and the third dielectric layer 13) , and having a distance D between the first and second trench patterns wherein D exceeds WS (see figs 6-7 for details);

h) anisotropically etching the first and second trench patterns through the third dielectric layer, thereby forming a first trench and a second trench, additional forming a third via pattern underlying the first trench and a fourth via pattern underlying the second trench (see figs 6-7 and col 5 lines 54-66 wherein the third dielectric 13 under the first and second trench patterns 15a being removed to form the first trench and the second trench respectively; and the third dielectric layer 13 located in the first and third opening 12a (counted from left to right) being etched by the first selective anisotropic etching (RIE) to form the third via pattern and the fourth via pattern respectively wherein the third and fourth via pattern respectively underlying the first and second trench); and

i) anisotropically etching the third and fourth via patterns through the first dielectric layer thereby forming the first via hole and the second via hole, wherein

[1] the first trench and the first via hole are adapted for forming a first dual damascene structure, and

[2] the second trench and the second via hole are adapted for forming a second dual-damascene

(see figs 6-7 and col 5 lines 54-66 wherein the first via hole (left opening 12b) being formed by etching the third via pattern through the first dielectric layer 4, and the

second via hole (right opening 12b) being formed by etching the third via pattern through the first dielectric 4).

- With respect to claim 23, Lin (figs 6-7 and col 5 lines 23-25, 46-48 & 54-56) discloses the first and third dielectric layer comprise materials having similar etching characteristics (the first dielectric layer comprising silicon oxide 4 while the third dielectric layer comprising silicon oxide 13, the first dielectric layer and the second dielectric layer are etched by the first selective RIE).

- With respect to claim 28, Lin (fig 5, col 5 lines 29-43) discloses depositing the first mask (11, photoresist) comprises depositing a mask layer selected from the group consisting of photoresist mask layers, hard mask layers, and combinations of photoresist layers and hard mask layers.

- With respect to claim 29, Lin (fig 8, col 6 lines 9-25) discloses simultaneously filling [1] the first trench and the first via hole, and [2] the second trench and the second via hole with a conductive material whereby first and second dual damascene structures are formed.

- With respect to claim 30, Lin (fig 8, col 6 lines 9-25) discloses the conductive material comprises one or more materials selected from the group consisting of metals, alloys, metallic superconductors and nonmetallic superconductors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13 and 15-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] in view of Inohara et al [US 5,976,972].

- With respect to claim 13, Lin, figs 4-8 and col 1-6, substantially discloses the claimed method of forming a structure on a substrate comprising step of:

a) forming a dielectric stack (3/4/10a, fig 4, col 5 lines 10-28) including an etch stop(10a);

b) depositing a first mask layer (11, fig 5, col 5 lines 29-34) on the etch stop layer wherein the first mask includes:

[1] a first via pattern having a width WV1 (see first opening between the first mask layer 11 being counted from left to right, fig 5),

[2] a second via pattern having a width WV2 (see the third opening between the first mask layer 11 being counted from left to right, fig 5), and

[3] a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS (see the second opening between the first mask layer 11 being counted from left to right, fig 5);

c) anisotropically etching the first and second via patterns through the etch stop layer thereby extending the first and second via patterns through the etch stop and forming a sacrificial etch segment by anisotropically etching the sacrificial etch pattern through the etch stop layer (see fig 5, col 5 lines 29-34);

d) forming the first trench on the etch stop layer such that the first trench does not overlay the sacrificial etch segment and wherein the first trench has a width WT1 (see the left trench 15b that does not overlay the sacrificial etch segment in fig 7);

e) forming a second trench having a width WT2 on the etch stop layer such that:

[1] the second trench does not overlay the sacrificial etch segment,

[2] the sacrificial etch segment is positioned between the first and second trenches,

[3] the distance between the first and second trenches exceeds WS (see the right trench 15b that does not overlay the sacrificial etch segment wherein the distance between the left and right trenches 15b exceeding the sacrificial etch pattern's width in fig 7);

f) forming a first via hole (left via hole 12b, fig 7) underlying the first trench (the left trench 15b) such that the first via hole communicates with the first trench and with the first via pattern extending through etch stop layer (10b); and

g) forming a second via hole (right via hole 12b, fig 7) underlying the second trench (the right trench 15b) such that the second via hole communicates with the second trench and with the second via pattern extending through the etch stop layer (10b) wherein [1] the first trench and the first via hole, and [2] the second trench and the second via hole areas adapted for forming a first dual damascene structure and a second dual damascene structure respectively.

Lin does not teach: **[a]** the first trench's width WT1 being narrower than the first via pattern's width WV1; and **[b]** the second trench's width WT2 being narrower than the second via pattern's width WV2.

However, Inohara et al (figs 28-31, col 12 lines 60-67, col 13 lines 1-60 and col 19 lines 10-15) teaches that using the trench pattern (46) with a width narrower than the width of the via pattern (51) would prevent reduction in contact area between the contact plug in the via hole and the upper wiring in the trench of the dual-damascene structure, even when misalignment occurs in lithographing step of forming the dual damascene structure.

Therefore, it would have been obvious for those skilled in the art to modify the process of Lin by using the first trench width WT1 and the second trench width WT2 as being claimed in **[a]** and **[b]**, per taught by Inohara et al, to provide the dual-damascene structure with a good interconnection wherein the problem of reduction in contact area is prevented even though misalignment occurs when forming the dual damascene structure.

- With respect to claim 15, the claimed range distance between the first and second trenches exceeding WS by at least 0.02μ is considered to involve routine optimization which has been held obvious to those skilled in the art . The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable

unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

- With respect to claim 16, Lin (fig 4, col 5 lines 10-27) discloses the etch stop layer comprises one or more dielectric materials selected from the group consisting of silicon oxides, silicon nitrides and silicon carbides.

- With respect to claim 17, Lin (fig 8, col 6 lines 9-25) discloses simultaneously filling the first and second trenches, and the first and second via holes with a conductive material (whereby first and second dual damascene structures are formed.

- With respect to claim 18, Lin (fig 8, col 6 lines 9-25) discloses the conductive material comprises one or more materials selected from the group consisting of metals, alloys, metallic superconductors and nonmetallic superconductors.

5. Claims 6, 7-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inohara et al [US 5,976,972] as applied to claim 1 above, in further view of Applied Materials Inc., "Applied Materials Announces Breakthrough low K dielectric film for High-Speed Cooper Chips", Business Wire, 10/6/1998, pp 1072 and Zhao et al, "A Cu/Low-k Dual Damascene Interconnect for High Performance and Low Cost Integrated Circuits", VLSI Technology 1998, Digest of Technical Paper 1998 Symposium, pp 28-29.

- With respect to claim 6, Inohara et al substantially discloses the claimed method including depositing a second mask layer (47, fig 29, col 13 lines 24-36) on the third dielectric,wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P such that T exceeds P a measure M. Inohara et al does not expressly teach the measure M being at least 0.2 microns. However, the claimed range of the measure M is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

- With respect to claims 7-8 and 10, Inohara et al substantially discloses the claimed method including using the second dielectric layer comprising one or more materials selected from the group consisting of silicon nitrides, silicon oxides and silicon carbides. Inohara et al does not expressly teach using the first and third dielectric layers comprising Black Diamond ™, amorphous fluorinated carbon, organic spin-on material, spin-on glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers or divinyl siloxane benzocyclobutane. However, these are materials having low k dielectric constants that has been known in the art to form dual damascene structure. See Zhao et al and Applied Materials Inc.'s documents as evidences. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." (65 USPQ at 301.). Therefore, it would have been obvious for those skilled in the art to select known low k dielectric materials as being claimed for the first and third dielectric layers in the process of Inohara et al to form a device with better interconnection wherein the improvement in speed and cross-talk noise is provided due to interconnect capacitance reduction.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inohara et al as applied to claim 11 above, and further in view of Inanaka et al [US 4,954,480].

Inohara et al substantially discloses the claimed method including simultaneously filling the second trench (46) and the via hole (48) with a conductive material whereby a dual damascene structure is formed. Inohara et al is silent about the usage of the conductive material comprises one or more materials selected from the group consisting of metallic superconductors and non metallic superconductors having zero direct current resistance at or below their superconducting transition temperature. However, using the conductive material comprises one or more materials selected from the group consisting of metallic superconductors and non metallic superconductors having zero direct current resistance at or below their superconducting transition temperature has been known in the art of forming interconnection in semiconductor device. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." (65 USPQ at 301.) See Inanaka et al that shows the usage of the superconductor material in forming interconnection structure. It would have been obvious for those skilled in the art to modify the process of Inohara et al by using the conductive material comprising superconductors as being claimed, per taught by Inanaka et al, to provide an interconnection structure with high conductivity wherein electrical resistance being of zero. By doing so, an interconnection structure with a high speed conduction and low time delay or degrade of signal will be formed.

7. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] as applied to claim 19 above, and in further view of Applied Materials Inc., "Applied Materials Announces Breakthrough low K dielectric film for High-Speed Cooper Chips", Business Wire, 10/6/1998, pp 1072 and Zhao et al, "A Cu/Low-k Dual Damascene Interconnect for High Performance and Low Cost Integrated Circuits", VLSI Technology 1998, Digest of Technical Paper 1998 Symposium, pp 28-29.

- With respect to claim 24, Lin substantially discloses the claimed method including depositing a second mask layer (14, fig 6) including a first trench pattern and a second trench pattern wherein a distance D between the first and second trench patterns exceeds the width WS of the sacrificial etch pattern (see figs 6-7 for details). Lin does expressly teach D exceeding WS by at least 0.2 μ. However, the claimed range of value of D exceeding WS is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious. See also In re Waite 77 USPQ 586 (CCPA1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

- With respect to claims 25-27, Lin substantially discloses the claimed method including using the second dielectric layer comprising one or more materials selected

from the group consisting of silicon nitrides, silicon oxides and silicon carbides. Lin does not expressly teach using the first and third dielectric layers comprising Black Diamond ™, amorphous fluorinated carbon, organic spin-on material, spin-on glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers or divinyl siloxane benzocyclobutane. However, these are materials having low k dielectric constants that has been known in the art to form dual damascene structure. See Zhao et al and Applied Materials Inc.'s documents as evidences. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." (65 USPQ at 301.) Therefore, it would have been obvious for those skilled in the art to select known low k dielectric materials as being claimed for the first and third dielectric layers in the process of Lin to form a device with better interconnection wherein the improvement in speed and cross-talk noise is provided due to interconnect capacitance reduction.

Response to Arguments

Applicant's Arguments in Paper No. 17 dated 12/18/01 have been fully considered and are not persuasive.

- Regarding to Applicant's argument in pages 6-13 about anticipation of reference Inohara et al, Applicant argues that "depositing a first dielectric layer **on** the substrate"

has a meaning of "the first dielectric layer is in contact with the substrate. If a cap layer is interposed between the first dielectric layer and the substrate, ...the first dielectric layer cannot be in contact with the substrate.....etching the second via pattern through the first dielectric layer thereby forming a via hole extending to the substrate would be inoperable". The argument is not persuasive because the first dielectric layer can be indirectly contact the substrate through the cap layer wherein the cap layer being interposed between the first dielectric layer and the substrate. The via hole extending to the substrate (the via hole in a direction toward to the substrate) can be formed by etching the second via pattern through the first dielectric layer. Moreover, when Applicant claims "depositing a first dielectric layer **on** the substrate", term "on" used as a function word to indicate position proximity with or direction/location with respect to something (See Merriam-Wester's Collegiate Dictionary), the first dielectric layer being on the substrate does not mean that the first dielectric layer has to be on and physical directly contact with the substrate (except the claim positively cites such limitation). Anyway, based on the ground rejection of claim 1 by Inohara et al of figs 28-31, the first dielectric layer 43 is deposited on the substrate 54/41/42 wherein the dielectric layer 43 is on and physical directly contact with the substrate 54/41/42. Claims 1, 9 and 10-11 are still anticipated by Inohara et al.

Regarding to Applicant's argument to claim 5, Applicant argues that claim 5 includes limitations of claim 1 with further limitation of (2) the substrate including at least one interconnect line, (3) depositing the first dielectric layer on the substrate and contacting the interconnect line wherein the dielectric layer is deposited without any

material interposed between the dielectric layer and the interconnect line. The argument is not persuasive because claim 5 does not cite limitation of depositing the first dielectric layer on the substrate and contacting the interconnect line wherein the dielectric layer is deposited without any material interposed between the dielectric layer and the interconnect line.

- Regarding to Applicant's argument on page 16 about the anticipation of claim 19 by Lin et al, Applicant argues that claim 19 includes limitation that the widths of the first and second trenches is narrower than the width of the first and second via etch pattern respectively. The argument is not persuasive because claim 19 does not include limitation of the widths of the first and second trenches being narrower than the width of the first and second via etch pattern respectively.

In addition, Applicant agrues that Lin does not teach forming sacrificial etch segment as being claimed in claim 19. The argument is not persuasive because Lin does teach forming sacrificial etch segment by anisotropically etching the sacrificial etch pattern through the second dielectric layer 10b (fig 5). According to figs 5-6, this sacrificial etch segment is located between the silicon nitride islands 10b where dual damascene structure is not formed. The purpose of this sacrificial etch segment is to reduce area of the silicon nitride islands (etch stop layer) in dual damascene fabrication for reducing unwanted capacitance. The purpose of sacrificial etch segment of the process of Lin is the same the purpose of the sacrificial etch segment of Applicant's invention.

Based on what being discussed above, claims 19, 23, and 28-30 are anticipated by Lin.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham Jr., whose telephone number is (703) 308-6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
April 4, 2003

SUPERVISORY PRIMARY EXAMINER
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